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EXAMINER	
JOHNSON, BRIAN P	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/715,688	SANDON ET AL.
	Examiner	Art Unit
	Brian P. Johnson	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16-24,26,27 and 29-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14, 16-24, 26, 27, 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-14, 16-24, 26-32 have been examined.

Acknowledgment of papers filed: amendments and remarks on June 14th, 2006. The papers filed have been placed on record. Examiner additionally acknowledges that the finality of the office action mailed on 23 August 2006 has been removed. This action has been made final and contains all current rejections and objections. Several objections in said previous action have been removed and the rejection with respect to claim 26 has been altered to maintain the original rejection from the office action mailed 14 March 2006.

Specification

2. The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Examiner suggests amending the current title back to the original title. Examiner withdraws the objection to the original title.

Claim Objections

Claim 26 objected to because of the following informalities: line 3 of claim 26 is written, "providing the processor" and would perhaps be better written as "providing a processor" to avoid any issues with regard to antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Rejection is withdrawn.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 8, 18, 20, and 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Van Hook (U.S. Patent No. 5,812,147).

5. Regarding claim 1, Van Hook discloses a processor, comprising M independent vector register files, said M vector register files adapted to collectively store a matrix of L data elements (fig 2A),

Note that registers in a particular column are considered to be a register file.

Each data element having B binary bits, said matrix having N rows and M columns, said L=N*M, each column having K subcolumns.(fig 2A—see below),

Said N.gtoreq.2, said M.gtoreq.2, said K.gtoreq.2, N=K*M,

Said B.gtoreq.1, each row of said N rows being addressable, each subcolumn of said K subcolumns being addressable (col 4 lines 41-55),

Note that each element of the matrix in fig 2A is accessible and, therefore, addressable. It follows that each column, row, and sub-column is also

addressable—in particular, they are accessed by a series of bits considered to be an address.

said processor not adapted to duplicatively store said L data elements. Note: examiner directs Applicant's attention to figure 2A with regards to several of the limitations within claim 1. The vector register file of figure 2A has 32 rows (note that N=32 which is more than 2). Each word (see col 4 lines 41-55) within Fig 2A is considered to be a column (note that M=4 which is more than 2). There is also considered to be 8 subcolumns per row, wherein each subcolumn consists of one word in width and 4 registers in height (note that K=8 which is more than 2). It follows that N=K*M (32=8*4). As stated previously, each element L is accessible through a series of bits (or, addressable) and, therefore, each of these macro-elements (in particular, N, K and M) are also addressable).

6. Regarding claim 2, Van Hook discloses the processor of claims 1, wherein the processor further comprises M address registers (fig. 2A), wherein each address register of the M address registers is associated with a corresponding one of the M vector register files (col 4 lines 41-55),

Wherein each of the M vector register files includes an array of N registers (col 2 lines 4-6), wherein each of the N*M registers of the M vector register files are adapted to store a data element of the L data elements (fig. 2A), and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file (col 4 lines 41-55).

7. Regarding claims 3, Van Hook discloses the processor of claims 2 and 10, wherein the data elements of each subcolumn are adapted to be stored in different vector register files, and wherein the data elements of each row are adapted to be stored in different vector register files (col 1 lines 40-45).

Note that, as with most any register file, there are no limitations to rearranging the information stored in memory. Using storing and load instructions, any set of information can be stored in a plurality of different configurations within the register file.

8. Regarding claims 4, Van Hook discloses the processor of claims 3 and 11, wherein the data elements of each subcolumn are adapted to be stored in different relative register locations of the different vector register files, and wherein the data elements of each row are adapted to be stored in a same relative register location of the different vector register files (col 2 lines 23-26).

See claims 3 and 11.

9. Regarding claim 8, Van Hook discloses the processor of claim 1, wherein the matrix of L data elements are stored in the M vector register files.

See claim 1.

10. Regarding claim 18, Van Hook discloses a processor, comprising M independent vector register files, said M vector register files adapted to

collectively store a matrix of L data elements, each data element having B binary bits (see claim 1), said matrix having N rows and M columns, said L=N*M (fig 2A and col 4 lines 41-55), each column having K subcolumns, said N.gtoreq.2, said M.gtoreq.2, said K.gtoreq.2, said N=K*M said B.gtoreq.1, each row of said N rows being addressable, each subcolumn of said K subcolumns being addressable (see claim 1),

Said matrix including a set of arrays such that each array is a row or subcolumn of the matrix (fig 2A), said processor adapted to execute an instruction that performs an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to the data elements of the first array (col 2 lines 24-28).

11. Regarding claim 20, Van Hook discloses the processor of claims 18 and 25, wherein the processor further comprises M address registers, wherein each address register of the M address registers is associated with a corresponding one of the M vector register files (see claim 1),

Wherein each of the M vector register files includes an array of N registers, wherein each of the N*M registers of the M vector register files are adapted to store a data element of the L data elements (fig 2A), and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file (col 4 lines 41-55).

12. Regarding claim 22, Van Hook discloses the processor of claim 18, wherein the instruction is adapted to rearrange the data elements of the first array within the first array.

Examiner asserts that a vector register file, like the one disclosed in Van Hook, is clearly able to rearrange its data.

13. Regarding claim 23, Van Hook discloses the processor of claims 18 and 25, wherein the processor is not adapted to duplicatively store the L data elements.

Note that the data elements are not required to be duplicatively stored in Van Hook.

14. Regarding claim 24, Van Hook discloses the processor of claim 18, wherein the matrix of L data elements are stored in the M vector register files.

See claim 1.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 5-7, 9-14, 16, 17, 19, 26, 27, and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook (U.S. Patent No. 5,812,147) in view of Gostin (U.S. Patent No. 5,832,290).

17. Regarding claims 5 and 13, Van Hook discloses the processor of claims 3 and 11, wherein the processor further comprises M multiplexers respectively coupled to the M vector register files (note that the selectivity of loading/storing requires multiplexers for each row/column, see col 4 lines 41-55),

And wherein if the matrix is stored in the M vector register files (fig 2A—see claim 1)then: the M multiplexers are adapted to respond to a command to read a row of the matrix by mapping the data elements of the row from the M vector register files to the row of the matrix in accordance with a read-row mapping algorithm (col 2 lines 24-28); and the M multiplexers are adapted to respond to a command to read a subcolumn of the matrix by reading the data elements of the subcolumn from the M vector register files to the subcolumn of the matrix in accordance with a read-subcolumn mapping algorithm.

Note that, with little clarification in Applicant's specification, the "write subcolumn mapping algorithm" and "write-row mapping algorithm" are considered to be no more than the logic necessary to allow the subcolumn and rows, respectively, to be adequately accessed.

Van Hook fails to disclose that a hardware multiplexer is used to control the vector processor.

Examiner asserts that it is just shy of inherent that a multiplexer as described in Applicant's claims is used to control the vector register file. Most every processor uses this technique; however, in case there is an exception overlooked by Examiner, these rejections will be obvious rejections.

Gostin discloses a vector register file controlled by a multiplexer (col 5 lines 1-5).

Van Hook, a computing system with a large variety of ways to access it's register file, would be clearly motivated to use a simple, fast, and widely tested technique of using a common multiplexer to control its vector register file.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the vector register file of Van Hook to utilize a multiplexer of Gostin which, as suggested by Gostin's use of a multiplexer, would utilize a binary switch to output binary values.

18. Regarding claims 6 and 14, Van Hook/Gostin discloses the processor of claims 3 and 11, wherein the processor further comprises M multiplexers respectively coupled to the M vector register files (see claim 5);

Wherein each multiplexer of the M multiplexers comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexer consists of the composite value of said binary bits (see claim 5),

Wherein the M multiplexers are adapted to respond to a command to write a row of the matrix by mapping the data elements of the row to the M vector

register files in accordance with a write-row mapping algorithm; and wherein the M multiplexers are adapted to respond to a command to write a subcolumn of the matrix by mapping the data elements of the subcolumn to the M vector register files in accordance with a write-subcolumn mapping algorithm.

Note that,similar to claim 5, with little clarification in Applicant's specification, the "write subcolumn mapping algorithm" and "write-row mapping algorithm" are considered to be no more than the logic necessary to allow the subcolumn and rows, respectively, to be adequately accessed.

19. Regarding claim 7, Van Hook/Gostin discloses the processor of claims 2 and 10, wherein the processor further comprises M multiplexers respectively coupled to the M vector register files such that each of the M multiplexers has a different value, wherein each multiplexer of the M multiplexers comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexer consists of the composite value of said binary bits (see claim 5)

20. Regarding claims 9-12, see claims 1-4.

21. Regarding claim 16, Van Hook/Gostin discloses the method of claim 9, further comprising addressing a row of the N rows (col 4 lines 41-55—see claim 1).

22. Regarding claim 17, Van Hook/Gostin discloses the method of claim 9, further comprising addressing a subcolumn of the K*M subcolumns (col 4 lines 41-55—see claim 1).

23. Regarding claim 19, Van Hook/Gostin discloses the processor of claims 18 and 25, wherein the processor further comprises M multiplexers respectively coupled to the M vector register files (see claim 5), wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits, and wherein the values associated with the M multiplexers control said selectivity (see claim 5).

exist in this invention, is considered to include a multiplexor for each element.

24. Regarding claims 27, 29, 30, 31 and 32, Van Hook discloses the limitations of claim 26: Van Hook discloses a method for processing matrix data, comprising:

A processor (col 3 lines 42);

M independent vector register files within the processor (fig 2A—see claim 1), said M vector register files collectively storing a matrix of L data elements, each data element having B binary bits, said matrix having N rows and M columns, said L=N*M, each column having K subcolumns said N is greater than or equal to 2, said M is greater than or equal to 2, said K is greater than or equal

to 1, said B is greater than or equal to one, each row of said N rows being addressable, each subcolumn of said K subcolumns being addressable, said matrix including a set of arrays such that each array is a row or subcolumn of the matrix (see claim 1 for explanation), and

Executing an instruction by said processor, said instruction performing an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to data elements of the first array (col 2 lines 24-28); and

Providing M multiplexers respectively coupled to the M vector register files, wherein the values associated with the M multiplexers control said selectivity (see claim 5).

25. Particularly regarding claims 27, 29, and 30, see claims 20, 22 and 23 respectively.

26. Particularly regarding claim 31, see claim 1 where K is greater than or equal to 2.

27. Particularly regarding claim 32, see claim 5.

Note that the new grounds rejection for claims 26, 27, 29, 30, 31 and 32 were necessitated by the amendments. The limitations of claim 26 were required to be rejected in order to reject claims 31 and 32. Claims 27, 29 and 30 now contain the limitations in the originally filed claim 26 that were not present initially. The rejections of claims 26, 27, 29 and 30 are maintained below.

28. Claims 21 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook in view of AMD 64-bit Technology (herein AMD).

29. Regarding claim 21 and 28, Van Hook discloses the processor of claim 18 and 26 and the use of instructions utilizing the memory matrix (fig 2A).

Van Hook fails to disclose enough detail about the types of instructions used.

AMD discloses a vector-shift instruction being supported (page 135 last paragraph, second to last line) and a vector move instruction (page 137 section 4.2.5 first paragraph).

It is expected that one of ordinary skill in the art would have realized the advantages of utilizing a shift and move instruction. Both of these instructions are fairly standard in most instruction sets because they give the programmer the ability to rearrange and interchange vector registers in a single instruction, steps that are often times essential while programming software to be utilized on a processor. AMD even discloses that "Move instructions...are among the most frequently used instructions in 128-bit media procedures" (page 137 section 4.2.5 first three lines). Examiner asserts that shift instructions are also commonly utilized by programmers. For these reasons, Lawrie would be motivated to include these instructions in the instruction set of the referenced invention.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the processing system of Van Hook to include vector-move and vector-shift instructions in order to have instructions that "insert an exact copy of the first array into the second array" and "rearrange the data elements of the first array within the first array", respectively.

Note: similar to claims 27, 29 and 30, a new grounds rejection for claim 28 appears appropriate since it did not contain the limitations of originally filed claim 26. However, the original rejection of claim 28 is maintained below.

Maintained Rejections

Claims 26, 27 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Access and Alignment of Data in an Array Processor (herein Lawrie).

30. Regarding claim 26, Lawrie discloses a processor, comprising M independent vector register files (page 99 introduction paragraph 1), said M vector register files adapted to collectively store a matrix of L data elements (page 99 section II second paragraph), each data element having B binary bits, said matrix having N rows and M columns, said L=N*M (page 99 section II second paragraph line 3), each column having K subcolumns (page 108 lines 11-14), said N.gtoreq.2, said M.gtoreq.2 (page 99 section II second paragraph line 3), said K.gtoreq.1, said B.gtoreq.1, each row of said N rows being addressable (page 99 section II second paragraph lines 4-6), each subcolumn of said K subcolumns being addressable (page 108 lines 11-14),

See claim 1.

Said matrix including a set of arrays such that each array is a row or subcolumn of the matrix (fig 2), said processor adapted to execute an instruction

that performs an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to the data elements of the first array (page 99 introduction paragraph 1).

Lawrie also discloses the processor of claims 18 and 25, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files, and wherein the values associated with the M multiplexors control said selectivity (page 100 col 1 second paragraph).

Note that, according to Wordnet ® 2.0 © 2003 Princeton University, a multiplexor is "a device that can interleave two or more activities"; therefore, the mechanism used to choose what values are put into the register file, a mechanism that must

31. Regarding claim 27, Lawrie discloses the processor of claim 26, wherein the processor further comprises M address registers (page 99 and 100 section II), wherein each address register of the M address registers is associated with a corresponding one of the M vector register files (page 108 lines 11-14),

Note that the rows are accessible, suggesting they are addressable, further suggesting that there is an "address register" for each register file (or row).

Wherein each of the M vector register files includes an array of N registers (page 99 and 100 section II), wherein each of the N*M registers of the M vector register files are adapted to store a data element of the L data elements (page 99 and 100 section II), and wherein each vector register file is independently

addressable through its associated address register being adapted to point to one of the N registers of said vector register file (page 108 lines 11-14).

32. Regarding claim 30, Lawrie discloses the processor of claim 26, wherein the processor is not adapted to duplicatively store the L data elements (page 100 fig 2).

33. Claims 28 and 29 rejected under 35 U.S.C. 103(a) as being unpatentable over Lawrie in view of AMD 64-bit Technology (herein AMD).

Regarding claims 28, Lawrie discloses the processor of claim 26 and the use of instructions utilizing the memory matrix (page 99 introduction).

Lawrie fails to disclose enough detail about the types of instructions used.

AMD discloses a vector-shift instruction being supported (page 135 last paragraph, second to last line) and a vector move instruction (page 137 section 4.2.5 first paragraph).

It is expected that one of ordinary skill in the art would have realized the advantages of utilizing a shift and move instruction. Both of these instructions are fairly standard in most instruction sets because they give the programmer the ability to rearrange and interchange vector registers in a single instruction, steps that are often times essential while programming software to be utilized on a processor. AMD even discloses that "Move instructions…are among the most frequently used instructions in 128-bit media procedures" (page 137 section 4.2.5 first three lines). Examiner asserts that shift instructions are also commonly

utilized by programmers. For these reasons, Lawrie would be motivated to include these instructions in the instruction set of the referenced invention.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the processing system of Lawrie to include vector-move and vector-shift instructions in order to have instructions that "insert an exact copy of the first array into the second array" and "rearrange the data elements of the first array within the first array", respectively.

Response to Arguments

34. Applicant's arguments with respect to claims 1-24 and 30 have been considered but are moot in view of the new ground(s) of rejection. Arguments with respect to claim 26 are addressed below.

35. Applicant states:

"Applicant's respectfully contend that Examiner's arguments are misdirected, because claim 26 recites that the M multiplexors are respectively coupled to the M vector register files, whereas the Examiner is arguing that the M multiplexors are respectively coupled to individual elements in a single register file. Applicants assert that Lawrie does not teach M multiplexors respectively coupled to the M vector register files."

Examiner disagrees and directs Applicants attention to the comment made with respect to claim 1, "Note that registers in a particular column are considered to be a register file." Examiner contends that this is a broad, but reasonable interpretation.

36. Applicant states:

"Applicants acknowledge that Lawrie, page 99, introduction, paragraph 1 teaches performing an operation with selectivity with respect to the data elements of the first array, as stated by the Examiner. However, Lawrie does not teach that said selectivity is controlled by the values associated with the M multiplexors."

Examiner disagrees. It has been argued that the selectivity requires the use of a "multiplexor". Additionally, Examiner asserts that computers do not selectively make choices arbitrarily; they require values to be checked.

37. Applicant states:

"Lawrie does not anticipate claim 26, Lawrie does not teach the feature: 'each row of said N rows being addressable"....[Examiner] merely states that any row can be accessed. However, a row can be accessed by addressing each individual element of the row and does not require addressing the row as a unit. Lawrie does not teach that the row as a unit is addressable. In addition, Lawrie does not teach a mechanism or algorithm for addressing a row as a unit. By not teaching a mechanism or algorithm for addressing a row as a unit, Lawrie's disclosure is non-enabling for addressing a row as a unit."

Examiner disagrees. The fact that a row can be accessed requires it to be addressable. To access a row, a certain number of bit values are required to be established to determine which row is being accessed. These bit values are considered to be an address. Additionally, Examiner asserts that one of ordinary skill in the art would have known how to address a row of a matrix without a particular "algorithm" disclosed in detail.

38. Applicant states:

"As a fourth example of why Lawrie does not anticipate claim 26, Lawrie does not teach the features: 'each subcolumn of said K subcolumns being addressable'. Lawrie's disclosure is specific to whole columns of the matrix to be stored and does not concern itself with individual subcolumns of a column such that each column has at least two subcolumns."

Examiner disagrees. If the columns are addressable, the subcolumns are addressable since they are being accessed using the same address as the column itself.

Conclusion

39. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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